

**N channel 60V MOSFET**

## 1. Description

The HS3205T is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

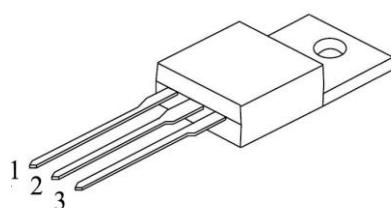
## 2. Feature

- $R_{DS(ON)} \leq 6.5\text{m}\Omega @ V_{GS} = 10\text{V}$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

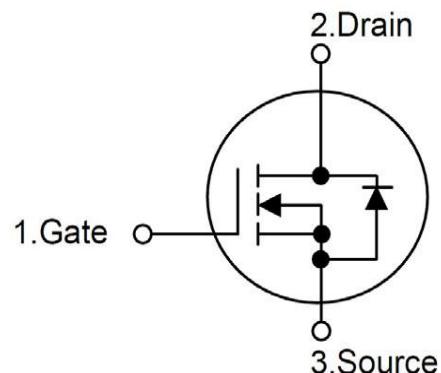
V <sub>DS</sub>	60	V
R <sub>DS(on)</sub>	6.5	$\text{m}\Omega$
I <sub>D</sub>	105	A

## 3. Pin configuration

Order Number	Package
HS3205T	TO-220



**TO-220**



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**4. Absolute maximum ratings (Tc=25°C Unless Otherwise Noted)**

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V <sub>DSS</sub>	60	V
Gate-Source Voltage		V <sub>DSS</sub>	±20	V
Continuous Drain Current	T <sub>c</sub> =25°C	I <sub>D</sub>	105	A
	T <sub>c</sub> =70°C		88	A
Pulsed Drain Current		I <sub>DM</sub>	419	A
Power Dissipation	T <sub>c</sub> =25°C	P <sub>D</sub>	200	W
	T <sub>c</sub> =70°C		140	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>Stg</sub>	-55 to 175	°C

**5. Thermal characteristics**

Parameter	Symbol	Ratings	Units
Thermal resistance, case-to-sink typ.	R <sub>thCS</sub>	0.5	°C/W
Thermal resistance junction to case.	R <sub>thJC</sub>	0.75	°C/W
Thermal resistance junction to ambient.	R <sub>thJC</sub>	62.5	°C/W

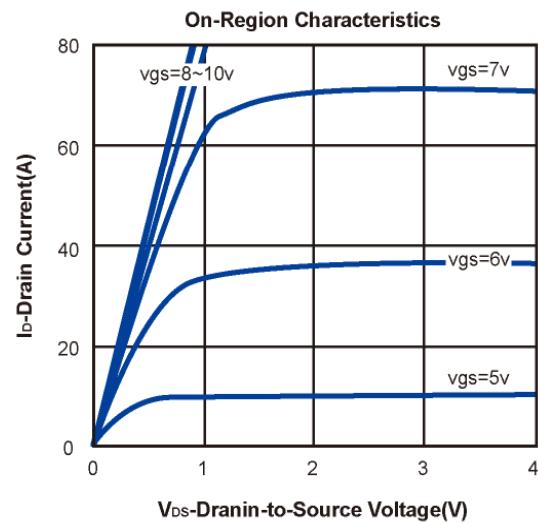
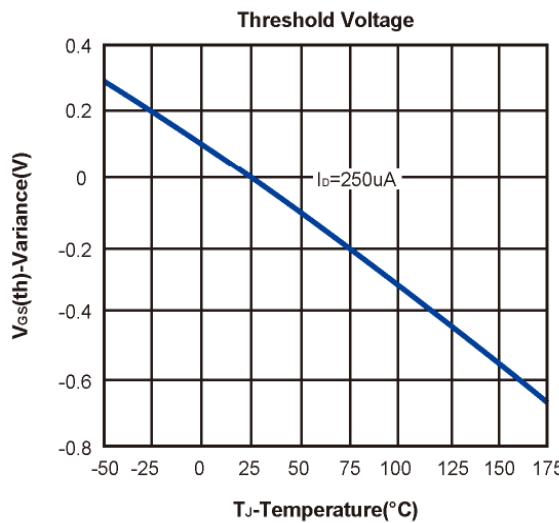
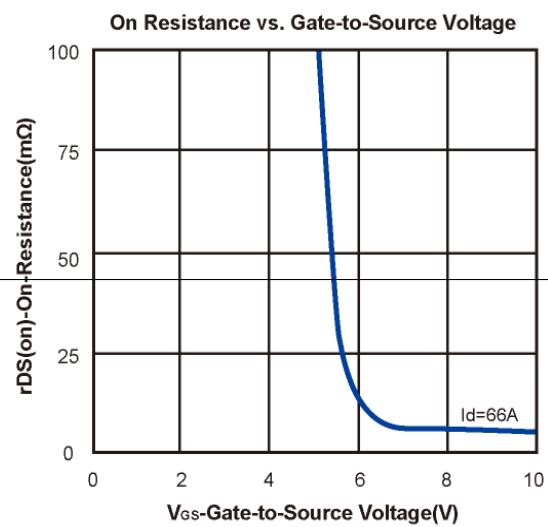
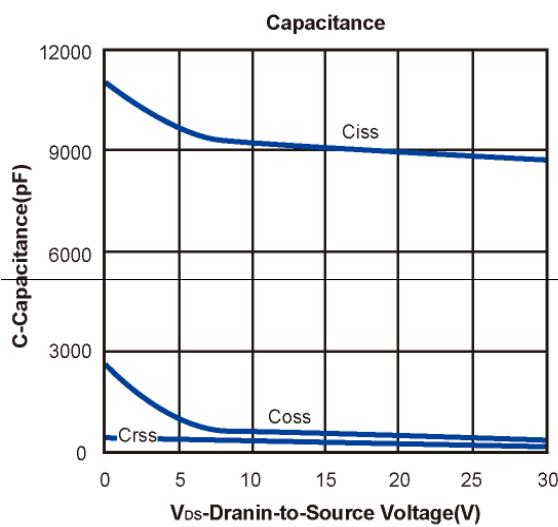
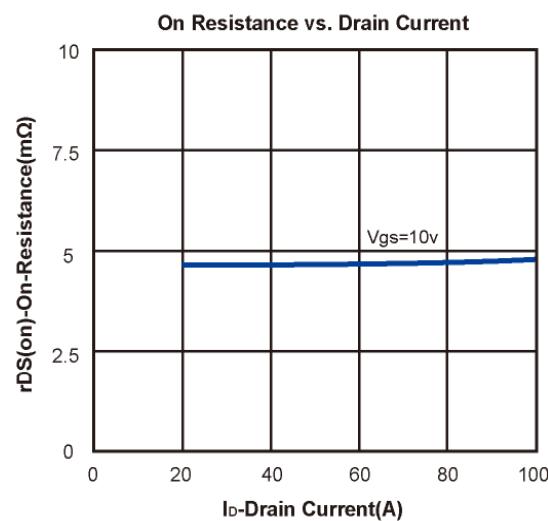
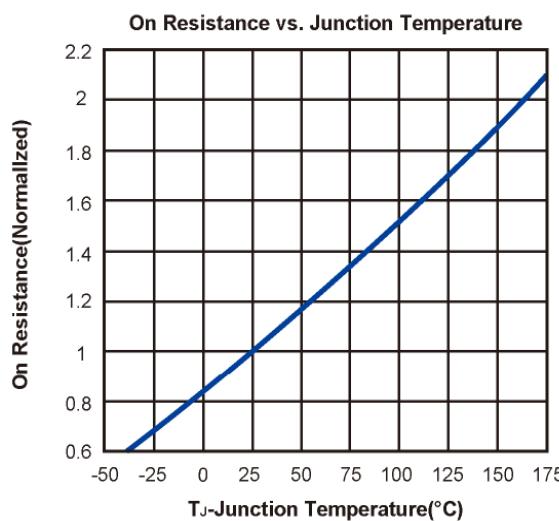
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**6. Electrical characteristics ( $T_A = 25^\circ\text{C}$  Unless Otherwise Specified)**

Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60	-	-	V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2	-	4	V
I <sub>GSS</sub>	Gate-Body Leakage	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V	-	-	±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	-	-	1	μA
R <sub>Ds(ON)</sub>	Drain-Source On-Resistance*	V <sub>GS</sub> =10V, I <sub>D</sub> =40A	-	4.9	6.5	mΩ
V <sub>SD</sub>	Diode Forward Voltage *	I <sub>S</sub> =40A, V <sub>GS</sub> =0V	-	-	1.3	V
<b>DYNAMIC</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DD</sub> =44V, V <sub>GS</sub> =10V, I <sub>D</sub> =66A	-	133	-	ns
Q <sub>gs</sub>	Gate-Source Charge		-	42.5	-	
Q <sub>gd</sub>	Gate-Drain Charge		-	40.5	-	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz	-	8793	-	pF
C <sub>oss</sub>	Output Capacitance		-	361	-	
C <sub>rss</sub>	Reverse Transfer Capacitance		-	193	-	
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =10V, R <sub>L</sub> =30Ω V <sub>DD</sub> =28V, R <sub>G</sub> =6.8Ω I <sub>D</sub> =66A	-	60.9	-	ns
t <sub>r</sub>	Turn-On Rise Time		-	219	-	
t <sub>d(off)</sub>	Turn-Off Delay Time		-	114	-	
t <sub>f</sub>	Turn-Off Fall Time		-	34.3	-	

Notes :a. pulse test:pulse width 300 us,duty cycle 2% ,Guaranteed by design,not subject to production testing.

b. HOMSEMI reserves the right to improve product design,functions and reliability without notice.

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